

PATENT

REMARKS

This paper is responsive to the final Office Action dated November 19, 2004. Claims 1-31 were examined. Applicant has cancelled claims 5, 9 – 20, 25, 27, 29, and 31. Applicant has amended claims 1, 21, 26, and 28.

Rejections under 35 U.S.C. §102

Claims 1-3, 5, 8-12, 14, 17, 19, 20, 21, 23, 24, and 26-31 are rejected under 35 U.S.C. §102(a) and (b) as being anticipated by U.S. Patent No. 5,881,264 issued to Kurosawa (hereinafter "Kurosawa"). Claims 5, 9 – 12, 14, 17, 19, 20, 27, 29, and 31 have been cancelled. The remaining rejected claims include 1 – 3, 8, 21, 23, 24, 26 – 28, and 30. Claims 1, 21, 26, and 28 have been amended. Applicant respectfully submits that the addresses in Kurosawa are not scoreboard indices and that the indices of Kurosawa are not utilized as recited in Applicant's claims.

The Office contends that such subject matter is disclosed in Kurosawa at column 6, lines 33 – 52 and Figure 3. Figure 3 depicts a plurality of scoreboard tables. According to the text at column 6, lines 23 – 36, Figure 3 depicts the following:

The entry number 102 is used to distinguish entries in the scoreboard. The operation code 103 is an entry for holding the type of an operation that the processor 1 requests (e.g., "Read" means a read operation and "Write" means a write operation). The address 103 is an entry for holding a memory address to be accessed. The completion flag 104 indicates the issuing of the operation has been completed. In the valid flag 107, a flag V (Valid) is set when the corresponding entry is valid and a flag I (Invalid) is set when the corresponding entry is invalid. In other words, the entry corresponding to flag V will be issued in the future and the entry corresponding to flag I is an empty entry that is not issued.

The remaining portion of the section relied upon by the Office discloses generation of addresses, and setting of synchronization flags. Although Kurosawa discloses scoreboard indices as seen in the above quoted section, these indices are not utilized to identify and invalidate entries in the scoreboard. Kurosawa does not disclose or suggest using the scoreboard indices to identify and invalidate. Kurosawa does not explicitly disclose how entries are selected and invalidated. Kurosawa only discloses that "[a]fter processing of the memory access instruction has been

PATENT

completed, the memory controller 10 sets to "T" the valid flag stored in the entry for the executed memory access instruction in the scoreboard..." (col. 9, lines 1 – 5). In fact, the disclosure of Kurosawa suggests that Kurosawa steps through the table (col. 9, line 10 – col. 11, line 50).

The Office also supports rejection of the claims by interpreting Kurosawa's addresses as scoreboard indices. Interpreting the addresses of Kurosawa as scoreboard indices both glosses over the terms utilized by Applicant in the claims and conflicts with the disclosure of Kurosawa, which already has indices. Furthermore, Kurosawa specifically discloses using the addresses to select a scoreboard and then accessing an invalid entry of the selected scoreboard, and does not disclose or suggest using the addresses for selecting a scoreboard entry and invalidating the selected entry (col. 8, lines 40 – 43).

For at least the reasons above, Kurosawa does not anticipate any of claims 1 – 3, 8, 21, 23, 24, 26 – 28, and 30. Therefore, claims 1 – 3, 8, 21, 23, 24, 26 – 28, and 30 are allowable over the art of record.

Rejections under 35 U.S.C. §103

Claims 4, 6, 7, 13, 15, 16, 18, 22 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kurosawa in view of U.S. Patent No. 6,473,832 issued to Ramagopal et al (hereinafter "Ramagopal"). Claims 13, 15, 16, 18, and 25 have been cancelled. The remaining rejected claims include claims 4, 6, 7, and 22. Applicant respectfully submits that these claims are allowable, at least because they depend from corresponding ones of the above allowable independent claims. In addition, claim 21 has been amended to recite a load-store unit.

Applicant respectfully submits that combining or modifying Kurosawa with Ramagopal still does not disclose or suggest Applicant's claims. The indices in Kurosawa only appear in the scoreboards and in the synchronization table (Figure 3). The scoreboard indices are never communicated to a load-store unit. Simply adding a load-store unit from Ramagopal to Kurosawa does not suddenly achieve forwarding or receiving a scoreboard index to/from a load-store unit as recited in claims 6 and 7, respectively. Such a combination or modification also does not disclose or suggest "locating an entry in a scoreboard for an instruction with a scoreboard index returned from a load-store unit" as recited in claim 21. Applicant respectfully

PATENT

submits that a combination or modification still must disclose or teach every limitation of the claims. The combination or modification performed by the Office does not satisfy this requirement. Adding the disclosure of Ramagopal to Kurosawa provides nothing more than a load-store unit.

Moreover, Applicant does not comprehend the supposed motivation for combining Kurosawa and Ramagopal provided by the Office. The Office states the following:

It would have been obvious to one of ordinary skill in the art to use Ramagopal in Kurosawa for including the indication of load data and forwarding (or receiving) the index value and the instruction to the load/store unit as claimed because the use of Ramagopal could provide Kurosawa the capability of the control circuit to adapt to particular access conditions of a given load or store instruction, thereby reducing the processing overhead of the control p[rocessor (sic) of Kurosawa, and it could be readily done by configuring the read/write port of load/store unit of Ramagopal into Kurosawa with modified control parameters, such as the port width and data type, so that the load/store unit of Ramagopal could be recognized by Kurosawa in order to achieve the enhanced, in doing so provided a motivation.

Applicant cannot locate the evidentiary support for this contention by the Office. "It is never appropriate to rely solely on 'common knowledge' in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based" (MPEP 2144.03, *citing In re Zurko*, 258 F.3d 1379 (Fed. Cir. 2001)). "[A]n assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support" (MPEP 2144.03, *citing Id.*).


Neither Kurosawa nor Ramagopal, standing alone or in combination, disclose or suggest any of Applicant's claims, including claims 4, 6, 7, 21, and 22. For at least these reasons, Applicant's claims are allowable.

Conclusion

In summary, claims 1 – 4, 6 – 8, 21 – 24, 26, 28, and 30 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is

PATENT

respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

<u>CERTIFICATE OF MAILING OR TRANSMISSION</u>	
I hereby certify that, on the date shown below, this correspondence is being	
<input type="checkbox"/> deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
<input checked="" type="checkbox"/> facsimile transmitted to the US Patent and Trademark Office.	
 Steven R. Gilliam	<u>16-Mar-2005</u> Date

Respectfully submitted,



Steven R. Gilliam, Reg. No. 51,734
Attorney for Applicant(s)
(512) 338-6320
(512) 338-6301 (fax)

EXPRESS MAIL LABEL: _____